REMARKS/ARGUMENTS

The Office Action (1) rejected claims 1, 3, 5, 7 and 8-11 under 35 U.S.C. 102(b) as being anticipated by Moon (5,744,374), (2) rejected claims 13, 15-19 under 35 U.S.C. 102(e) as being anticipated by Sakai et al. (2003/0067022), (3) rejected claims 2 and 6 under 35 U.S.C. 103(a) as being unpatentable over Moon in view of Willer et al. (6,538,273), (4) rejected claims 4 and 12 under 35 U.S.C. 103(a) as being unpatentable over Moon in view of Gnadinger (6,674,110), (5) rejected claim 14 under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. in view of Willer et al., and (6) rejected claim 20 under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. in view of Gnadinger.

To address the specific rejections of the examiner:

1. Regarding claims 1, 3, 5, 7 and 8-11 under 35 U.S.C. 102(b) as being anticipated by Moon (5,744,374), applicant submits that these claims are not anticipated by Moon due to the disclosure of a *conductive oxide layer* overlying the semiconductor substrate in the present invention ferroelectric transistor, different from Moon's yttrium oxide *dielectric layer*. The present invention ferroelectric transistor design thus comprises a semiconductor substrate, *a conductive oxide layer*, a ferroelectric layer and a conductive layer, in that order. Instead, Moon's ferroelectric transistor design comprises a semiconductor substrate, *a yttrium oxide layer*, a ferroelectric layer and a conductive layer, in that order (claim 1, column 6, lines 65-67).

Applicant submits that the yttrium oxide layer of Moon's disclosure is a dielectric layer, and therefore markedly different from the present invention conductive oxide layer. Moon specifically discloses that yttrium oxide is used as a buffer dielectric film between the silicon semiconductor substrate and the ferroelectric film (column 4, lines 1-3, and column 6, lines 35-37).

Furthermore, the present invention ferroelectric transistor design exhibits significant improvements by employing a conductive oxide layer instead of a dielectric layer between the ferroelectric layer and the semiconductor substrate. A basic ferroelectric transistor is a MFS FET (Metal Ferroelectric Semiconductor Field Effect Transistor), comprising a Metal electrode on a Ferroelectric layer in contact with a Semiconductor surface. The basic difficulty of this design is the ferroelectric/semiconductor interface. When a ferroelectric film is deposited directly on the silicon substrate, metals and oxygen from the ferroelectric layer may diffuse into the ferroelectric-silicon interface, creating interface trap charges, affecting the polarization of the ferroelectric film, and overall may make the operation of the ferroelectric transistor becoming unstable. Further, since the thermal expansion coefficient and lattice structure of a ferroelectric film is not compatible with silicon, it is very difficult to form a high-quality ferroelectric film with a clean interface directly on the silicon substrate.

To solve the ferroelectric/semiconductor interface problem, an interfacial layer can be inserted between the ferroelectric and the semiconductor layers. If an insulator layer is used as an interfacial layer, the ferroelectric design is called a MFIS FET (Metal Ferroelectric Insulator Semiconductor Field Effect Transistor), having an Insulator sandwiching between the Ferroelectric and the Semiconductor. Similar transistor

operations can also be achieved with a Metal/Insulator interfacial multilayer to provide a MFMIS FET (Metal Ferroelectric Metal Insulator Semiconductor). Such ferroelectric transistor designs (MFIS FET and MFMIS FET) overcome the surface interface and surface state issues of a ferroelectric layer in contact with the silicon substrate. However, they incorporate other difficulties such as higher operation voltage and trapped charges in the bottom floating gate layer. The operation voltage of these transistors is higher than the ferroelectric layer programming voltage by an amount of the voltage across the gate dielectric. And when there is a voltage applied across the ferroelectric thin film, there will be current flow in the gate stack, and charges would be trapped in this floating electrode. The trapped charges may neutralize the polarization charges at the interface of the bottom electrode and the ferroelectric film and could shorten the memory retention time of this structure.

The disclosure of Moon is a ferroelectric memory transistor of the type MFIS FET with yttrium oxide acting as the insulator (column 1, lines 49-50, and described in first embodiment of column 4, line 43 and second embodiment of column 5, lines 47-48). The yttrium oxide of Moon can provide a good interface with the semiconductor substrate due to a possible lattice matching with the ferroelectric layer and therefore can provide a good quality ferroelectric film, but still needed higher operating voltage and still facing possible charge trapping degradation.

In contrast, the present invention discloses a conductive oxide interfacial layer. The ferroelectric transistor of the present invention is either MFCS FET (Metal Ferroelectric Conductive-oxide Semiconductor Field Effect Transistor) or MFMCS FET (Metal Ferroelectric Metal Conductive-

oxide Semiconductor Field Effect Transistor). By not using dielectric as the interface layer, the present invention MFCS and MFMCS FET can avoid the higher operating voltage and the possible charge trapping effect.

Thus applicant submits that the present invention MFCS FET and MFMCS FET are novel and cannot be anticipated with Moon's MFIS FET using yttrium oxide as insulator, not only because that Moon does not disclose a conductive oxide material on the semiconductor surface, but also since the conductive oxide material disclosed in the present invention MFCS and MFMCS FETs provides different and improved functionalities such as lower operation voltage function and reduced trapped charge problem associated with MFIS FET devices.

Applicant submits that based on the different interfacial material between the ferroelectric and the semiconductor surface (conductive oxide v. dielectric oxide), plus the additional advantages in lower operation voltage and less charge trapping degradation, the present disclosure cannot be anticipated by Moon.

2. Regarding claims 13, 15-19 under 35 U.S.C. 102(e) as being anticipated by Sakai et al. (2003/0067022), applicant has amended the claim to overcome the rejection by specifying that the conductive oxide layer is directly contacting the semiconductor substrate. Applicant submits that these amended claims are not anticipated by Sakai due to the disclosure of a *conductive oxide layer* directly overlying the semiconductor substrate in the present invention ferroelectric transistor, different from Sakai's first *insulator layer*. The present invention ferroelectric transistor design thus comprises a semiconductor substrate, *a conductive oxide layer*, a ferroelectric layer and a conductor layer, in that order. Instead, Sakai's ferroelectric transistor design comprises a semiconductor substrate, *a first insulator layer*, a first conductor layer, a ferroelectric layer and a second conductor layer, in that order (layer 3 of Fig. 1, abstract,

lines 7-9, paragraph 016, lines 6-9, claim 1, lines 5-8, claims 8-10, 12). In the disclosure of Sakai et al., the first insulator layer is always in direct contact with the semiconductor substrate. And similar to Moon, Sakai et al. disclose a ferroelectric transistor of the type MFMIS FET (paragraph 006), and therefore still needed higher operating voltage and still facing possible charge trapping degradation.

Applicant submits that the present invention MFCS FET and MFMCS FET are novel and cannot be anticipated by Sakai et al., not only because that Sakai et al. does not disclose a conductive oxide material in contact with the semiconductor surface, but also since the present invention MFCS and MFMCS FETs employing conductive oxide material in contact with the semiconductor surface provide different and improved functionalities such as lower operation voltage function and reduced trapped charge problem as compared with Sakai et al.'s MFMIS FET using an insulator layer in contact with a semiconductor substrate.

Thus applicant submits that based on the different contacting layer material to the semiconductor surface (conductive oxide v. insulator), plus the additional advantages in lower operation voltage and less charge trapping degradation, the present disclosure cannot be anticipated by Sakai et al.

3. Regarding claims 2 and 6 under 35 U.S.C. 103(a) as being unpatentable over Moon in view of Willer et al. (6,538,273), applicant submits that these claims are not anticipated and rendered obvious under Moon in view of Willer et al. due to the requirement of a Schottky diode formation (metal/semiconductor junction) of Willer et al.

Willer et al. disclose a metallic intermediate (conductor) layer deposited over a semiconductor, forming a metal/semiconductor junction of the Schottky diode (abstract, lines 3-5, column 2, lines 4-6, claim 1, lines 8-

11, claim 8, lines 6-9). Therefore, according to the teaching of Willer et al., a metal (conductor) layer has to contact a semiconductor layer (so that a Schottky diode can form). Thus applicant submits that it would not be obvious by following Willer et al.'s teaching to modify Moon by inserting a conductive layer between the conductive oxide layer and the ferroelectric layer because the conductive layer would not be in contact with the semiconductor layer and thus there is no conductive layer/semiconductor interface (i.e., no Schottky diode formation).

Further, the present invention conductive oxide layer provides advantages and improvements not realized in both Moon yttrium oxide dielectric layer and Willer et al. metallic layer. Willer et al. employs a different interfacial layer between a ferroelectric layer and a semiconductor substrate: a metallic layer forming a Schottky diode for the type of MFMS FET (Metal Ferroelectric Metal Semiconductor Field Effect Transistor). The MFMS FET design does not use a dielectric interface layer, thus does not have the problem of higher operating voltage nor the issue of charge trapping. However, the use of a metallic layer to form Schottky diode can have its own problematic complications. First of all, to form a Schottky diode, the metal and the semiconductor have to satisfy certain requirements such as the work function and the Fermi energy level. For example, for n type silicon semiconductor, the metal has to be selected so that the work function of the metal has to be higher than the Fermi level of the semiconductor. For p type silicon semiconductor, the metal is chosen so that the work function is lower. Thus the requirement of Schottky diode formation imposed by Willer et al. would restrict the selection of the metallic and semiconductor materials and doping species. In addition a Schottky

diode of the type metal/semiconductor interface is relatively leaky. The "OFF" current of the memory transistor with Schottky gate will be large. As a result no large array without large standby power consumption can be fabricated. Further, the MFMS FET requires the gate (metal/semiconductor Schottky diode) to be separated from N+ or P+ source drain junction. This is because it is not possible to fabricate a Schottky diode by a metal to heavily doped semiconductor surface because the metal to heavily doped semiconductor contact is an ohmic contact. This separation can result in low drive current of the MFMS FET design.

The present invention MFCS and MFMCS FET can have significant advantages over the MFMS FET design which uses metallic interfacial layer to form Schottky diode. The conductivity of a conductive oxide is not very high, and conductive oxide behaves more like a semiconductor. Thus the contact between the conductive oxide and the semiconductor can be a P/N junction, or a kind-of-ohmic N+/N or P+/P contact. The conductive oxide used in the present invention ferroelectric memory applications is designed to form a P/N junction with the silicon substrate. For example, indium oxide (InO_x) is n-type while the silicon is p-type. Also conductive oxide in general has large bandgap so that good Schottky diode with low leakage current can be fabricated to provide large array with low standby power consumption. Further, the present invention MFCS and MFMCS FET design provides a good low leakage current junction with heavily doped opposite type of semiconductor, thus can reduce or eliminate the separation problem associate with MFMS FET design.

Thus applicant submits that Moon taken in view of Willer et al. cannot anticipate and render these claims of the present invention obvious

due to the requirement of a Schottky diode formation of Willer et al., and the advantages of the conductive oxide/semiconductor interface as compared to the metallic/semiconductor interface (Schottky diode formation) of Willer et al.

4. Regarding claims 4 and 12 under 35 U.S.C. 103(a) as being unpatentable over Moon in view of Gnadinger (6,674,110), applicant submits that these claims are not anticipated by either Moon and Gnadinger due to the disclosure of a *conductive oxide layer* overlying the semiconductor substrate. Moon discloses only a yttrium oxide dielectric layer deposited over a semiconductor substrate. Gnadinger discloses an interfacial oxide dielectric layer between the ferroelectric and the semiconductor substrate.

Similar to Moon, the disclosure of Gnadinger is a ferroelectric memory transistor of the type MFIS FET with the insulator layer being the interfacial oxide of the ferroelectric layer. The Gnadinger ferroelectric memory design can reduce the higher operating voltage problem since the interfacial layer of Gnadinger has higher dielectric constant than silicon dioxide, and the ferroelectric material has lower dielectric constant than prior art ferroelectric material. However, since Gnadinger still employs a dielectric interface layer, the operating voltage is still higher than MFS FET design, and with the possibility of charge trapping degradation.

Thus the present invention conductive oxide layer provides advantages and improvements not realized in both Moon yttrium oxide dielectric layer and Gnadinger interfacial oxide layer. Applicant submits that based on the different interfacial material between the ferroelectric and the semiconductor surface (conductive oxide v. dielectric oxide), plus the additional advantages in lower operation voltage and less charge trapping

degradation, the present disclosure cannot be anticipated by Moon, even in view of Gnadinger.

5. Regarding claim 14 under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. in view of Willer et al., applicant submits that these claims are not anticipated by Sakai et al. in view of Willer et al. due to the requirement of a Schottky diode formation (metal/semiconductor junction) of Willer et al.

Thus similar to the above argument with respect to Moon in view of Willer et al., applicant submits that Sakai et al. taken in view of Willer et al. cannot anticipate and render these claims of the present invention obvious due to the requirement of a Schottky diode formation, and the advantages of the conductive oxide/semiconductor interface as compared to the metallic/semiconductor interface (Schottky diode formation) of Willer et al.

6. Regarding claim 20 under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. in view of Gnadinger, applicant submits that these claims are not anticipated by Sakai et al. due to the disclosure of a *conductive oxide layer* overlying the semiconductor substrate. Neither Sakai et al. nor Gnadinger disclose a conductive oxide layer overlying a semiconductor substrate. Sakai et al. disclose only a insulator layer deposited over a semiconductor substrate, and Gnadinger discloses an interfacial oxide dielectric layer between the ferroelectric and the semiconductor substrate.

Thus similar to the above argument with respect to Moon in view of Gnadinger, applicant submits that Sakai et al. taken in view of Gnadinger cannot anticipate and render these claims of the present invention

obvious due to the different interfacial material between the ferroelectric and the semiconductor surface (conductive oxide v. dielectric oxide), plus the additional advantages in lower operation voltage and less charge trapping degradation.

In summary, applicant submits that none of these references, singly or combination can anticipate nor can render claims 1-20 obvious.

This response is accompanied by a Petition for Extension of Time Under 37 C.F.R. §1.136(a) requesting a two-month extension, together with a deposit account authorization for the fee therefore.

In view of the foregoing, applicants request reconsideration of the application, as amended, and submit that the application is now in allowable form and should be passed to issue.

Respectfully submitted,

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